



## PATENT ABSTRACTS OF JAPAN

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**G11C 11/34**(21) Application number: **60002760**(71) Applicant: **NEC CORP**(22) Date of filing: **11.01.85**(72) Inventor: **SUGIMOTO MASUNORI**(54) **SENSE AMPLIFIER CIRCUIT**

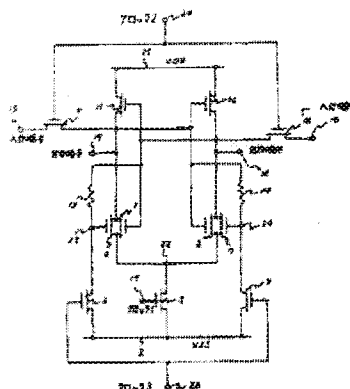
floating capacity small.

(57) Abstract:

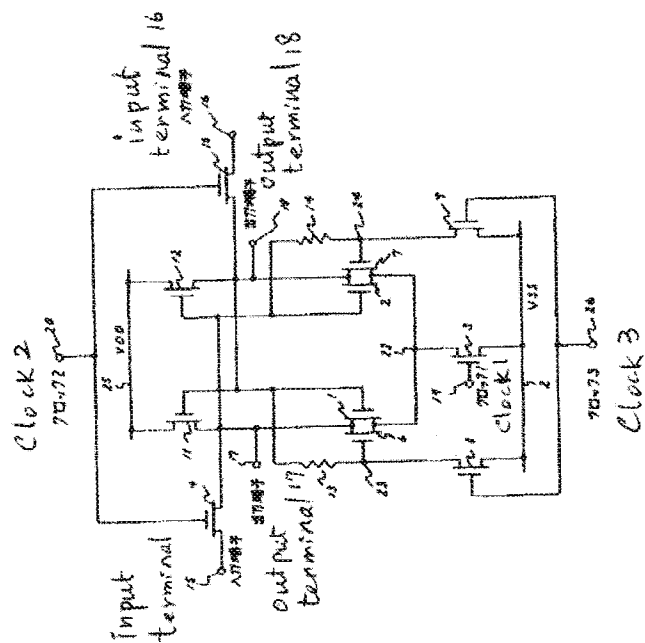
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**PURPOSE:** To obtain a sense amplifier circuit in which high speed operation is compatible with noise resisting property by combining MISFETs (metal insula tor semiconductor field effect transistor).

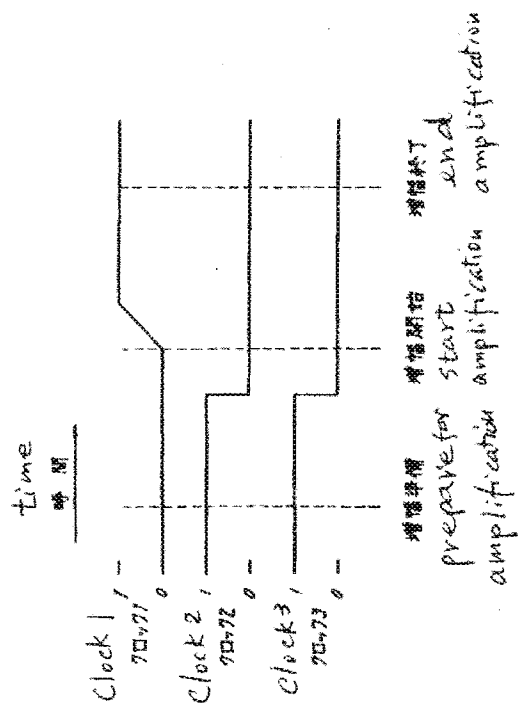
**CONSTITUTION:** Just before starting amplification, MISFET3 is cut off, MISFETs 4, 5 and 8, 9 are made conductive, and consequently, MISFETs 6, 7 are cut off and potential of output terminals 17, 18 are nearly equal to potential of input terminals 15, 16 respectively. At the time of amplification, MISFETs 4, 5 and 8, 9 are cut off, the potential of a clock terminal 19 is changed, and MISFET3 is made conductive. At the time of amplification, MISFETs 6, 7 are left disconnected, and no influence is given on operation. MISFETs 1, 2, 11, 12 constitute a flip-flop circuit, and amplify potential difference which was in output terminals 17, 18 by positive feedback action just before amplification, and one is made to VSS and another to VDD. At the time of amplification, only the floating capacity of output terminals 17, 18 has relevance, and the fast operation can be obtained by making this



第 1 图



第 2 图



R1 Q/E